

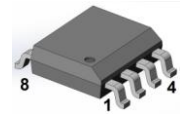
### Matched NPN transistor pair

#### Features

- "Ideal" and identical transistors
- Common-mode rejection ratio > 120dB
- Emitter-base offset voltage < 100μV
- Emitter-base offset voltage temperature drift 0,1μV/°C
- Current gain ( $h_{FE}$ ) matched < 2%
- Parameters are guaranteed in the range of collector current of 10μA to 1mA
- Noise Voltage Density of 1,8 nV /√Hz
- Ideal logarithmic properties

AS194H,  
AS394H,  
AS394CH

AS194DE  
AS394DE,  
AS394CDE



#### General Description

The AS194 and AS394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs.

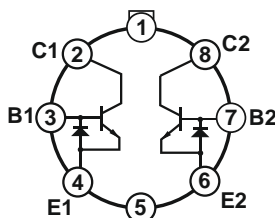
Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic base and emitter resistances is very low, giving very low noise and operating over a wide current range.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

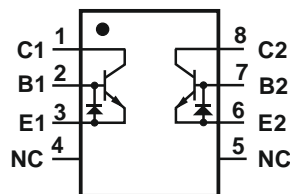
The AS194H, AS394H, AS394CH are available in the 8-pin metal can TO5-8 package and the AS394DE and AS394CDE in the 8-lead plastic SOIC-8 (150mil) EPAD package.

#### Connection Diagram

##### Top View



AS194H,  
AS394H,  
AS394CH  
Metal Can Package  
(TO5-8)



AS194DE  
AS394DE,  
AS394CDE  
SOIC-8 (150mil) / EPAD

#### Pin Information

Pins number Package type		Symbol	Description
TO5-8	SOIC-8/ EPAD		
1	4	NC	Not connected
2	1	C1	Collector1
3	2	B1	Base1
4	3	E1	Emitter1
5	5	NC	Not connected
6	6	E2	Emitter2
7	7	B2	Base2
8	8	C2	Collector2
	EPAD		Substrate

#### Absolute Maximum Ratings

- Collector Current 20mA
- Collector-Emitter Voltage AS194, AS394 40V  
AS394C 20V
- Collector-Base Voltage AS194, AS394 40V  
AS394C 20V
- Collector-Substrate Voltage AS194, AS394 40V  
AS394C 20V
- Collector-Collector Voltage AS194, AS394 40V  
AS394C 20V
- Base-Emitter Current 10mA



**Electrical performance characteristics**

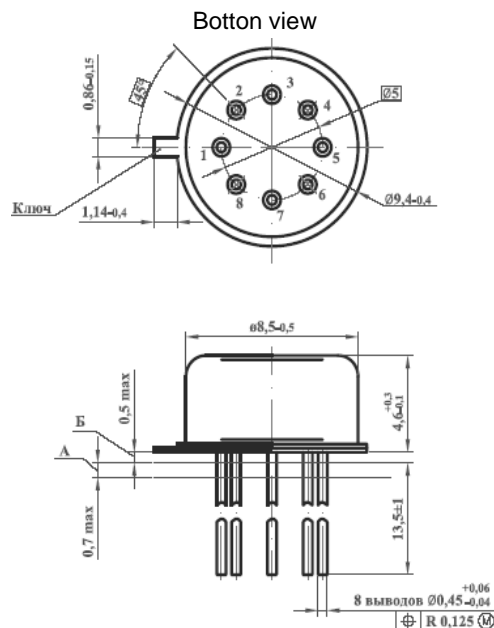
Parameter, units	Conditions	AS194H AS194DE			AS394H AS394DE			AS394CH AS394CDE		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
Current Gain ( $h_{FE}$ )	$U_{CB}=0\text{ V}$ до $U_{MAX}$ (Note1)									
	$I_C=1\text{ mA}$	350	700		300	700		250	500	
	$I_C=100\text{ }\mu\text{A}$	350	550		250	550		230	400	
	$I_C=10\text{ }\mu\text{A}$	300	450		200	450		150	300	
	$I_C=1\text{ }\mu\text{A}$		300			300			200	
Current Gain Match, $\Delta h_{FE\ 1,2} = 100[\Delta I_B] [h_{FE(MIN)}] / I_C, \%$	$U_{CB}=0\text{ V}$ to $U_{MAX}$ $I_C=10\text{ }\mu\text{A}$ to $I_C=1\text{ mA}$		0,5	2		0,5	4		1	5
Emitter-Base Offset Voltage, $\mu\text{V}$	$U_{CB}=0\text{ V}$ $I_C=10\text{ }\mu\text{A}$ to $I_C=1\text{ mA}$		25	100			150			200
Change in Emitter-Base Offset Voltage vs Collector-Base Voltage (CMRR), $\mu\text{V}$	(Note1) $I_C=10\text{ }\mu\text{A}$ to $I_C=1\text{ mA}$ $U_{CB}=0\text{ V}$ to $U_{MAX}$		10	25		10	50		10	100
Change in Emitter-Base Offset Voltage vs Collector Current, $\mu\text{V}$	$U_{CB}=0\text{ V}$ $I_C=10\text{ }\mu\text{A}$ to $1\text{ mA}$		5	25		5	50		5	50
Collector-Base Leakage, nA	$U_{CB}=U_{MAX}$		0,05	0,3		0,05	0,5		0,05	0,5
Collector- Collector Leakage, nA	$U_{CC}=U_{MAX}$		1	2			5			5
Input Voltage Noise, nV $\sqrt{\text{Hz}}$	$U_{CB}=0\text{ V}$ , $I_C=100\text{ }\mu\text{A}$ $f=100\text{ Hz} - 100\text{ kHz}$		1,8				1,8		1,8	
Collector to Emitter Saturation Voltage, V	$I_C=1\text{ mA}$ , $I_B=10\text{ }\mu\text{A}$		0,2	0,25	-	0,2	0,25		0,2	0,25
	$I_C=1\text{ mA}$ , $I_B=100\text{ }\mu\text{A}$		0,1	0,15	-	0,1	0,15		0,1	0,15

Note 1: Collector-base voltage is swept from 0 to  $U_{MAX}=35\text{V}$  at a collector current of  $10\text{ }\mu\text{A}$ ,  $100\text{ }\mu\text{A}$  and  $1\text{ mA}$ .

Note 2: Offset voltage drift with  $V_{OS}=0$  at  $T_A=25^\circ\text{C}$  is valid only when the ratio of  $I_{C1}$  to  $I_{C2}$  is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at  $+25\text{ }^\circ\text{C}$  and temperature extremes.

Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

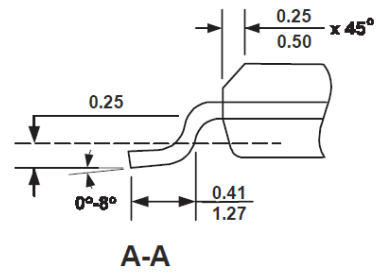
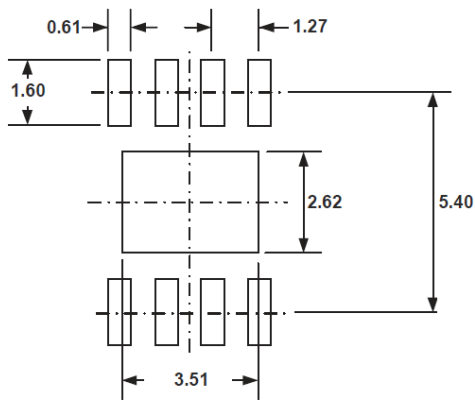
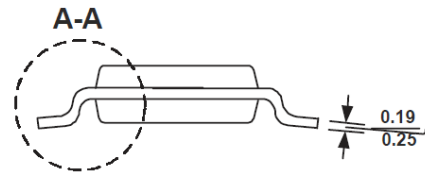
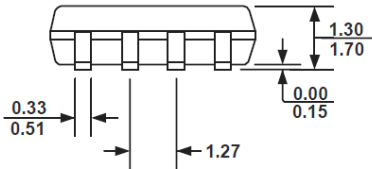
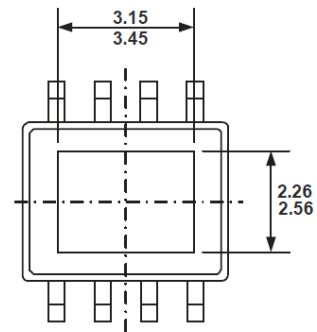
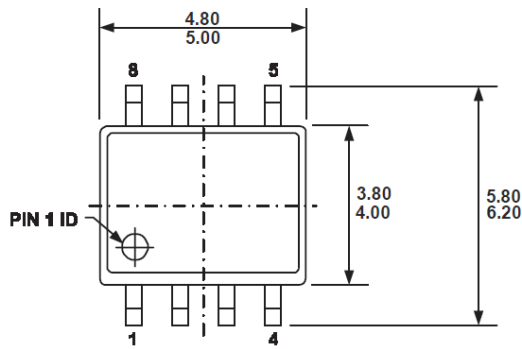
**Physical Dimensions in millimeters**



**8-lead TO-5 metal can package**



Physical Dimensions in millimeters (Continued)



SOIC-8 (150mil) EPAD